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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/689,312	10/20/2003	Mark Beaumont	DB001067-000	2868

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EXAMINER	
WAI, ERIC CHARLES	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/689,312	BEAUMONT, MARK	
	Examiner	Art Unit	
	Eric C. Wai	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *01/07/2004,10/20/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Information Disclosure Statement

2. The information disclosure statement filed 10/20/2003 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1-7, 11-14, 17, and 20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-7, 12-15, 18, and 21 of copending Application No. 10/689,355.

5. Although the conflicting claims are not identical, they are not patentably distinct from each other. For instance, claim 1 of copending Application No. 10/689,355 recites the same steps as claim 1 of the present application. The only difference is the substitution of "determining a running partial deviation sum" in the present application with the step of "determining a sum weighted deviation" in copending Application No. 10/689,355. It would have been obvious to one of ordinary skill in the art to use a sum weighted deviation. One would be motivated by the desire to have a greater variety of choices when performing the claimed load balancing method. .

6. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

7. Claims 1-9, and 11-17, and 20 are provisionally rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-8, 12-15, and 20 of copending Application No. 10/689,336. Although the conflicting claims are not identical, they are not patentably distinct from each other.

8. Although the conflicting claims are not identical, they are not patentably distinct from each other. For instance, claim 1 of copending Application No. 10/689,336recites

the same steps as claim 1 of the present application. The only difference is the substitution of "determining a running partial deviation sum" in the present application with the step of "determining a sum deviation" in copending Application No. 10/689,336. It would have been obvious to one of ordinary skill in the art to use a sum deviation in the determination to balance loads. One would be motivated by the desire to have a greater variety of choices when performing the claimed load balancing method.

9. This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Rejections - 35 USC § 101

10. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

11. Claim 20 recites a "memory device"; however, it appears that the system would reasonably be interpreted by one of ordinary skill in the art as software, per se, failing to be tangibly embodied or include any recited hardware as part of the system.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms are not clearly understood:

i. Claims 1, 11, and 20 recite, "determining a running partial deviation sum for each of said plurality of processing elements". It is unclear how this step relates to the rest of the invention (i.e. is the determining a transfer parameter performed on the basis of the partial deviation sum?).

ii. Claims 4 and 13 recite, "*V*". It is unclear what is meant by "*V*". Claims 4 and 13 also recite, "E_r". It is unclear how this value is derived for each of the plurality of processing elements. Claim 13 also recites, "PE_r" without providing a definition.

iii. Claim 5 recites, "wherein E_r controls said *Trunc* function." It is unclear how *Er* 'controls' the function. Furthermore, it is unclear how this step is possible since each E_r value is set ahead of time and must be different for each processing element as stated in claim 4.

iv. Claim 6 recites, "X and (X+1)". It is unclear what is meant by this.

v. Claim 8 recites, "transmitting ... to another of said plurality of processing elements within said loop". It is unclear whether the local deviation associated with each of said plurality of processing elements is sent to all the other processing elements or whether it is sent to just one

other processing element. Furthermore, it is unclear how the "another of said processing elements" is chosen.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith (US Pub No. US 2004/0024874 A1) in view of Wheat (US Pat No. 5,603,129).

16. Wheat was disclosed on IDS dated 10/20/2003.

17. Regarding claim 1, Smith teaches a method for balancing the load of a parallel processing system having a plurality of parallel processing elements arranged in a loop (Fig 1-3), wherein each processing element (PE_r) has a local number of tasks associated therewith, wherein r represents the number for a selected processing element, and wherein each of said processing elements is operable to communicate with a clockwise adjacent processing element and with an anti-clockwise adjacent processing element ([0039] and Fig 2, bi-directional link), the method comprising:

calculating a local deviation for each of said plurality of processing elements ([[0019]]);

determining a clockwise transfer parameter and an anti-clockwise transfer parameter for each of said plurality of processing elements ([0018-0020]); and

redistributing tasks among said plurality of processing elements in response to said clockwise transfer parameter and said anti-clockwise parameter for each of said plurality of processing elements ([0020]).

18. Smith does not teach the steps of determining a total number of tasks present within said loop; calculating a local mean number of tasks for each of said plurality of processing elements; determining a running partial deviation sum for each of said plurality of processing elements.

19. Wheat teaches a dynamic load balancing method by determining the average load across a processor array and minimizing a global imbalance or work loads within a finite number of balancing steps (col 6 lines 58-67).

20. It would have been obvious to one of ordinary skill in the art at the time of the invention to combine Smith and Wheat. One would be motivated by the desire to reduce the imbalance of workloads within a finite number of balancing steps as taught by Wheat.

21. Regarding claim 2, Wheat teaches that determining a total number of tasks present within said loop, comprises:

transmitting said local number of tasks associated with each of said plurality of processing elements to each other of said plurality of processing elements within said loop (col 5 lines 60-63);

receiving within each of said plurality of processing elements said number of local tasks associated with said each other of said plurality of processing elements (col 5 lines 60-63); and

summing said number of local tasks associated with each of said plurality of processing elements with said number of local tasks associated with each other of said plurality of processing elements (col 5 lines 55-56, wherein it is well known that the total number of tasks must be calculated to form an average).

22. Regarding claim 3, Smith and Wheat do not explicitly teach that said determining said total number of tasks present within said loop includes solving the equation $V = \sum_{i=0}^{i=N-1} v_i$,where N represents the number of said processing elements in said loop and v_i represents said local number of tasks associated with an i^{th} processing element in said loop.

23. Official notice is made that it is well known in the art to perform such a summation when calculating the number of tasks.

24. Regarding claim 4, Smith and Wheat do not teach calculating a local mean number of tasks within each of said plurality of processing elements includes solving the equation $M_r = Trunc((V+E_r)/N)$, where M_r is said local mean for said PE_r, N is the total number of said processing elements in said loop, and E_r is a number in the range of 0 to $(N-1)$ and wherein each processing element has a different E_r value.

25. Official notice is made that it is well known to perform a local mean calculation using this method and using a truncation function to remove unnecessary decimals. It would have been obvious to one of ordinary skill in the art at the time of the invention to also include a parameter to account for processing elements that have more processing capability. One would be motivated by the desire to ensure an equitable distribution.

26. Regarding claim 5, Smith and Wheat do not teach that E_r controls said *Trunc* function such that said total number of tasks for said loop is equal to the sum of the local mean number of tasks for each of said plurality of processing elements in said loop.

27. It would have been obvious to one of ordinary skill in the art at the time of the invention to change the value of E_r. One would be motivated by the desire to ensure that the sum of the local mean values do not exceed the total number of tasks.

28. Regarding claim 6, Smith and Wheat do not teach that said local mean M_r $=Trunc((V+E_r)/N)$ for each local PE_r within said loop is equal to one of X and (X+1).

29. It would have been obvious to one of ordinary skill in the art at the time of the invention that the local mean for each local PE_r within said loop is equal to one of X and (X+1).

30. Regarding claim 7, Smith and Wheat do not explicitly teach calculating a local deviation within each of said plurality of processing elements comprises finding the

difference between said local number of tasks for each of said plurality of processing elements and said local mean number for each of said plurality of processing elements.

31. It would have been obvious to one of ordinary skill in the art at the time of the invention to calculate a local deviation using this method. It is well known in the art that a deviation is defined as the difference between two values.

32. Regarding claim 8, Smith and Wheat do not teach determining a running partial deviation sum for each of said plurality of processing elements comprises:

transmitting said local deviation associated with each of said plurality of processing elements to another of said plurality of processing elements within said loop;

receiving within each of said plurality of processing elements said local deviation associated with at least one other of said plurality of processing elements; and

summing said local deviation associated with each of said plurality of processing elements with said local deviation associated with at least one other of said plurality of processing elements.

33. It would have been obvious to one of ordinary skill in the art at the time of the invention to calculate a partial deviation sum using this method. One would be motivated by the desire to perform a summation of all the local deviation values.

34. Regarding claim 9, Smith and Wheat do not teach determining a running partial deviation sum for each of said plurality of processing elements comprises solving the equation $S_j = \sum_{i=0}^{i=j} D_i$,where S_j represents said running partial deviation sum, D_i

represents the local deviation associated with the i^{th} processing element, and $j \neq (N-1)$ where N is the number of processing elements on said loop.

35. It would have been obvious to one of ordinary skill in the art at the time of the invention to calculate a partial deviation sum using this method. One would be motivated by the desire to perform a summation of all the local deviation values.

36. Regarding claim 10, Smith and Wheat do not explicitly teach determining a clockwise transfer parameter and an anti-clockwise transfer parameter within each of said processing elements comprises:

setting $T_a=(H_r+L_r)\div 2$; and

setting $T_c=D-T_a$ where H_r represents a highest extrema of said running partial deviation sum; L_r represents a lowest extrema of said running partial deviation sum, D represents the local deviation of a selected local processing element; and T_c represents said clockwise transfer parameter, and T_a represents said anti-clockwise transfer parameter.

37. Wheat teaches a balancing method where units of work are redistributed (col 7 lines 1-44). Wheat teaches that the units of work to be transferred (β) is determined according to the equations on col 7 lines 5-25. While Wheat does not teach using the highest and lowest extrema of the running partial deviation sum, it would have been obvious to one of ordinary skill in the art at the time of the invention to calculate utilize such values. One would be motivated by the desire to account for extremes in the total load deviation for the entire system.

38. Regarding claims 11-16, and 18-19, they are rejected for the same reasons as claims 1-2, 4-5, and 8-10 above.

39. Regarding claim 17, Wheat teaches that all the steps are completed simultaneously for each of said plurality of processing elements within said loop (col 5 lines 52-67, wherein each processor performs the load balancing).

40. Regarding claim 20, it is the memory device claim of claim 1 above. Therefore, it is rejected for the same reasons as claim 1 above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric C. Wai whose telephone number is 571-270-1012. The examiner can normally be reached on Mon-Thurs, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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